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| 10/039,777 | 12/31/2001 | Deborah T. Marr | 042390.P12495 | 9070 |

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| EXAMINER | |
|---|---|
| HUISMAN, DAVID J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/039,777 | MARR ET AL. | |
| | Examiner | Art Unit | |
| | David J. Huisman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06 March 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-26 have been examined.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 1/24/2006 and IDS as received on 3/6/2006.

### *Amendment Comments*

3. The examiner would like to point out a minor error in the amendment page headers for clarification purposes. In the amended specification and claims, and also in the remarks, applicant has identified the wrong application serial number (09864042), the wrong amendment date (06/23/05), and the wrong reply date (03/23/2005).

### *Drawings*

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "195" has been used to designate both the memory and thread 1 in Fig.1. According to paragraph [0016] of the specification, it appears that thread 1 should be assigned number "196". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

5. Claim 18 is objected to because of the following informalities: In he last paragraph, replace "proscessor" with --processor--. Appropriate correction is required.

### *Maintained Rejections*

6. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

### *Claim Rejections - 35 USC § 112*

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 24-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the examiner has been unable to locate any particular structure(s)

in the specification that perform(s) the relinquishing and/or re-partitioning of resources. And, one of ordinary skill in the art would not necessarily know what type of structure is capable of relinquishing/re-partitioning resources. Since applicant is claiming means for performing such functions, structures corresponding to those functions must be described. See MPEP 2163, part 3(a). If applicant believes that a structure is disclosed which performs the relinquishing and re-partitioning functions, then it is asked that applicant point out the structure in the specification.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 24-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 24 includes a means for relinquishing resources and a means for re-partitioning resources. It appears as though applicant discloses the functions of relinquishing and re-partitioning but discloses no express, implied or inherent disclosure of hardware or a combination of hardware and software that performs the functions. Therefore, the application has not disclosed any "structure" which corresponds to the claimed means. If applicant feels that a structure has been disclosed, applicant must describe at least one specific structure or material that corresponds to the claimed means in question, and to identify the precise location or locations in the specification where a description of at least one embodiment of that claimed means can be found. See MPEP 2106, section V, part A2.

***Claim Rejections - 35 USC § 102***

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-26 rejected under 35 U.S.C. 102(e) as being anticipated by Kalafatis et al., U.S. Patent Number 6,535,905 (as applied in the previous Office Action and herein referred to as Kalafatis).

14. Referring to claims 1 and 18 Kalafatis has taught a processor comprising: a memory to store a plurality of program threads (column 3, lines 61-65, and note the existence of main memory);

a plurality of thread partitionable resources that are each partitionable between a plurality of threads (Kalafatis figure 4; note that any combination of components including one of components 106, 62, 103, and retirement logic is a partitionable resource; column 13 lines 32-38);

a processor coupled to said memory being separate from said processor; See column 3, lines 61-65, and note main memory, which is a memory external to the processor.

logic to receive a program instruction from a first thread of said plurality of threads, and in response to said program instruction to cause the processor to suspend execution of the first thread and to relinquish portions of said plurality of thread partitionable resources associated with the first thread for use by other ones of said plurality of threads. See Kalafatis figure 14

figure 8 column 10 lines 25-39, column 18 lines 62-column 19 line 36; switching takes place between threads when a branch instruction occurs, and also at an instruction, or inserted flow, is inserted in the instruction sequence. For example, components 103, 72, and 70, of Fig.4, make up an overall partitionable resource. When thread 0 is active, thread 0 instructions are sent from the corresponding IQ partition to the execution unit. When thread 0 is suspended, for whatever reason, the execution portion of the resource is relinquished so that it may be used by thread 1 (or another thread if one exists).

15. Referring to claim 2 Kalafatis has taught wherein the program instruction is a suspend instruction which consists of a suspend opcode which explicitly directs the processor to suspend execution of the first thread and to relinquish portions of said plurality of thread partitionable resources associated with the first thread for use by other ones of said plurality of threads (Kalafatis figure 14, column 18 lines 62-column 19 line 36; switching takes place between threads when an instruction, or inserted flow, is inserted in the instruction sequence).

16. Referring to claim 3 Kalafatis has taught wherein said logic is to cause the processor to suspend the first thread for a selected amount of time (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63).

17. Referring to claim 4 Kalafatis has taught wherein said selected amount of time is a fixed amount of time (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63; the number is predetermined).

18. Referring to claims 5 and 19 Kalafatis has taught wherein said processor is to execute instructions from a second thread while said first thread is suspended (Kalafatis column 2 lines 3-12, column 4 lines 10-49).

19. Referring to claims 6 and 20 Kalafatis has taught wherein said selected amount of time is programmable by at least one technique chosen from a set consisting of:

providing an operand in conjunction with the program instruction; blowing fuses to set the selected amount; setting the selected amount in microcode (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-column 14 line 6; since the number is predetermined, it is programmable by the control register bus).

20. Referring to claims 7 and 21 Kalafatis has taught wherein said plurality of thread partitionable resources comprises: an instruction queue (Kalafatis figure 4 number 103); a register pool (Kalafatis column 13 lines 32-46).

21. Referring to claims 8 and 22 Kalafatis has taught further comprising: a plurality of shared resources, said plurality of shared resources comprising: a plurality of execution units (Kalafatis figure 4 number 70); a cache (Kalafatis figure 4 number 44); a scheduler (Kalafatis figure 4 number 72); a plurality of duplicated resources, said plurality of duplicated resources comprising: a plurality of processor state variables; an instruction pointer; register renaming logic (Kalafatis figure 4 number 76/78, 100).

22. Referring to claims 9 and 23 Kalafatis has taught wherein said plurality of thread partitionable resources further comprises: a plurality of re-order buffers; a plurality of store buffer entries (Kalafatis column 13 lines 32-46).

23. Referring to claim 10 Kalafatis has taught wherein said logic is further to cause the processor to resume execution of said first thread in response to an event (Kalafatis column 8 lines 5-36).

24. Referring to claim 11 Kalafatis has taught wherein said logic is further to cause the processor to ignore events until said selected amount of time has elapsed (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63; the number is predetermined).

25. Referring to claim 12 Kalafatis has taught wherein said processor is embodied in digital format on a computer readable medium (Kalafatis column 1 line 5-column 2 line 15).

26. Referring to claims 13 and 24 Kalafatis has taught a method comprising:

receiving a first opcode in a first thread of execution;

suspending said first thread for a selected amount of time in response to said first opcode;

relinquishing a plurality of thread partitionable resources in response to said first opcode (Kalafatis figure 14 figure 8 column 10 lines 25-39, column 18 lines 62-column 19 line 36; switching takes place between threads when a branch instruction occurs (i.e., branch opcode is detected), and also at an instruction, or inserted flow, is inserted in the instruction sequence). For example, components 103, 72, and 70, of Fig.4, make up an overall partitionable resource. When thread 0 is active, thread 0 instructions are sent from the corresponding IQ partition to the execution unit. When thread 0 is suspended, for whatever reason, the execution portion of the resource is relinquished so that it may be used by thread 1 (or another thread if one exists).

re-partitioning said plurality of resources after a selected amount of time (Kalafatis column 10 lines 62-column 11 line 19, column 7 lines 8-35). For example, again taking components 103, 72, and 70, of Fig.4, as a resource, it can be seen that when thread 0 is active, then the resource is partitioned such that the thread-0 portion of the IQ, the

scheduler, and the execution unit, are all assigned to operating on thread 0, whereas the thread-1 portion of the IQ is assigned to thread 1. When thread 1 becomes active, the resource is repartitioned such that the thread-1 portion of the IQ, the scheduler, and the execution unit, are all assigned to operating on thread 1, whereas the thread-0 portion of the IQ is assigned to thread 0. Then, ultimately, when thread 0 becomes active again, the resource is repartitioned such that the thread-0 portion of the IQ, the scheduler, and the execution unit, are all assigned to operating on thread 0, whereas the thread-1 portion of the IQ is assigned to thread 1.

27. Referring to claim 14 Kalafatis has taught wherein relinquishing comprises: annealing the plurality of thread partitionable resources to become larger structures usable by fewer threads (Kalafatis column 7 lines 8-35, figure 2).

28. Referring to claims 15 and 26 Kalafatis has taught wherein relinquishing said plurality of thread partitionable resources comprises: relinquishing a partition of an instruction queue(Kalafatis figure 4 number 103) ; relinquishing a plurality of registers from a register pool (a register pool (Kalafatis column 13 lines 32-46).

29. Referring to claim 16 Kalafatis has taught wherein relinquishing said plurality of thread partitionable resources further comprises: relinquishing a plurality of store buffer entries; relinquishing a plurality of re-order buffer entries (Kalafatis column 13 lines 32-46).

Referring to claim 17 Kalafatis has taught wherein said selected amount of time is programmable by at least one technique chosen from a set consisting of:

providing an operand in conjunction with the first opcode;

blowing fuses to set the selected amount of time;

programming the selected amount of time in a storage location in advance of decoding the program instruction;

setting the selected amount of time in microcode (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-column 14 line 6; since the number is predetermined, it is programmable by the control register bus).

30. Referring to claim 25 Kalafatis has wherein said first instruction is a macro-instruction from a user-executable program (Kalafatis column 3 line 45-column 4 line 7).

***Response to Arguments***

31. Applicant's arguments filed on January 24, 2006, have been fully considered but they are not persuasive.

32. Applicant argues the 112 rejection of claims 24-26 on page 11 of the remarks, in substance that:

> "Claims 24-26 were rejected under 35 U.S.C. 112 (first & second paragraphs). Applicants respectfully traverse the rejection because paragraph 22 (page 9) clearly identifies that the partition/anneal logic (1 14) of FIG.1 as being the logic for relinquishing and partitioning the resources. Based on this revision, Applicants respectfully request the Examiner to withdraw the outstanding 112 rejections."

33. These arguments are not found persuasive for the following reasons:

a) Applicant had previously argued that claim 24 invokes 112, 6$^{th}$ paragraph, due to the means+function language of the claim. In this case, the specification must disclose a structure that performs the claimed function. After looking through applicant's specification, the item which performs the claimed function is shown as a box labeled as "partition/anneal 114" in Fig.1, and is referred to as partition/anneal logic. However, there are no details regarding the structure of such a component. Everything in a computer system can inherently be labeled as

logic without specifying structure. For instance, I could say that I have logic to predict branches. However, this does not imply some structure such as a 2-bit prediction counter or a branch target buffer. Similarly, it is not clear what applicant expects his claimed means to be interpreted as because no structure has been disclosed. Instead, just logic for performing the function is disclosed. This logic could be anything (software or hardware).

34. Applicant argues the novelty/rejection of claims 13 and 24 on page 11 of the remarks, in substance that:

> "...the Examiner has failed to identify where Kalafatis provides teaching for (1) "receiving a first opcode in a first thread of execution" and "suspending said first thread for a selected amount of time in response to said opcode," and (2) "means for receiving a first instruction from a first thread" and "means for suspending said first thread in response to said first instruction.""

35. These arguments are not found persuasive for the following reasons:

a) As pointer out in the rejection of claims 13 and 24, Fig.4 and the specified passages discloses receiving instructions/opcodes and suspending execution of a particular thread for a period of time.

36. Applicant argues the novelty/rejection of claim 1 on page 12 of the remarks, in substance that:

> "Applicants respectfully submit that Kalafatis does not describe logic to receive a program instruction from a first thread directing said processor to suspend execution ...and to relinquish portions of said plurality of thread partitionable resources associated with the first thread for use by other ones of said plurality of threads. Emphasis added. Herein, the Examiner states that the components (103, 72, 70) make up an overall partitionable resource. See Page 6 of the Office Action. However, there is no teaching of suspending execution of the first thread and relinquishing of portions of these alleged "partitionable resources" in response to the program instruction."

37. These arguments are not found persuasive for the following reasons:

a) Instructions are inherently received by logic. And, some instruction cause a processor to suspend execution of a given thread and relinquish the resources associated with the given thread. See column 10, lines 25-39 or column 18, line 62, to column 19, line 36. Looking at Fig.8, if the conditions set forth in steps 226, 248, and 260 are satisfied, then a branch instruction will cause a switch from thread 0 to tread 1. This causes the processor to suspend execution of thread 0 and the resources currently used to process thread 0 will be relinquished so that they may be used to process thread 1.

38. Applicant argues the novelty/rejection of claim 18 on page 12 of the remarks, in substance that:

> "With respect to independent claim 18, Applicants respectfully submit that Kalafatis does not describe the memory that is separate from the processor and used to store the program threads. This is in direct contrast to the buffer and queues set forth in FIG. 4 of Kalafatis, which are selected components of microprocessor."

39. These arguments are not found persuasive for the following reasons:

a) In addition to instructions (of threads) being stored in cache and buffers/queues, instructions are also stored in main memory, which is known to be separate from the processor. See column 3, lines 61-65.

40. Applicant argues the novelty/rejection of claim 18 on page 12 of the remarks, in substance that:

> "With respect to claims 3-4, 6, 11, 16, and 20, the Examiner relies on text within column 22 of Kalafatis. It is respectfully asserted that it is impermissible to rely on the language in the claims as support for the teachings of Kalafatis. The scope of a patent's claims determines what infringes a patent; it is no measure of what it discloses. In re Benno, 768 F2d 1340, 226 USPQ 683, 686 (Fed.Cir.1985). Thus, the rejection is impermissible. It is respectfully requested that the Examiner identify the specific areas in the specification where Kalafatis describes those alleged limitations."

41. These arguments are not found persuasive for the following reasons:

a) It is not clear why relying on at least some claim language is impermissible. As is known, the claims are part of the disclosure, and since all patents are presumed to be valid (35 U.S.C. 282), the claims are fully supported and enabled by the specification. In addition, in examining In re Betto, it appears that this case is only relevant when the question is obviousness. However, the examiner has made all 102 rejections, and the elements in the claim cited are actually present.

***Conclusion***

42. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
March 20, 2006

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